RT-Simex addresses the general challenge of improving methods and tools for the design of embedded software. Its goal is the development of techniques to relate different predictions and observations of real-time software behaviour. Expected behaviours and timing constraints will be formalized in a design model with the standard UML/MARTE. Observations (simulation and execution) will be recorded by « execution traces », provided by several execution environments: Real-time Java, LinuxRT, general purpose processor. Interpretation of data will be done by an analysis of static information (model based design, reverse-engineered code) and by graphic representations in order to help testing, validation, or debug activities.

TECHNOLOGICAL OR SCIENTIFIC INNOVATIONS

- Real time design by extending existing modelers (Papyrus and Obeo Designer) for UML design and Marte timing analysis.
- Provide an unify trace format and extending real-time platforms.
- Eclipse analysis platform for dynamic, static and design feedbacks.

STATUS - MAIN PROJECT OUTCOMES

- Step 1: Choice a Marte methodology for design and analysis, definition of an unify trace format.
- Step 2: Improve tooling for observability of execution platform by customize code generators, create architecture configurators or improve real time engines.
- Step 3: improve reverse engineering tooling to support runtime traces, static code analysing and create debugging graphical view points compliant with Marte designers.
- The RT-Simex platform now allows to graphically specify timing constraints on activity diagrams and sequence diagrams, and to view the flow execution of any realtime program, whatever the used runtime.
- By creating a bridge between the trace format, Timesquare and Obeo Designer, we will allow a step-by-step debugging and a timing violation analysis directly at the design model.

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PROJECT DATA

Coordinator:
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Call:
ANR

Start date:
September 2009

Duration:
36 months

Global budget (M€):
2.1

Funding (M€):
1